

Power switch ROMs and PROMs quickly and safely with a simple circuit that reduces the turn-on and turn-off delay and keeps your data intact.

Most TTL-based ROMs and PROMs can be operated by applying power only when you actually want to access the information they hold. But you must take some precautions if you want to operate successfully in this mode.

Examine the power switch in Fig. 1. If the input is taken to ground either through a switch or through the output of a TTL gate, base current flows through R_1 to turn on the pnp transistor. If the input is allowed to float or be pulled high by a TTL output, resistor R_2 turns the transistor off.

When the pnp transistor turns on, the V_{CC} terminal of the ROM rises rapidly to a voltage just below that of the V_{CC} supply. The difference is determined by the V_{CE} (SAT) of the pnp transistor. When the transistor is turned off, the V_{CC} for the ROM decays to a low value (Fig. 2). Turn-on time is how long it takes for the input signal to propagate through the switch and raise V_{CC} to the 4-V level, at which most ROMs and PROMs are fully functional—even though not all the device specs may be met.

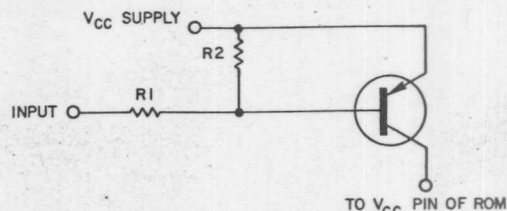
Now it's time to propagate

Once the device's V_{CC} has reached 4 V, time is required for all inputs to propagate through the device and establish the correct output state. This is true regardless of whether the inputs are stable before V_{CC} is switched on, or whether V_{CC} and the inputs are switched at the same time.

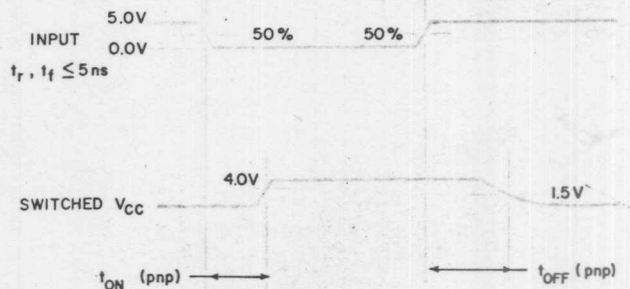
The required propagation time is approximately t_{AA} , the address-access time given in the data sheets. Typically, ROMs and PROMs reach the correct state within 20 ns of the specified t_{AA} . So the "worst-case enable time" of a power-switched device is given as follows:

$$t_{enable} = t_{on(pnp)} + t_{AA} + 20 \text{ ns.} \quad (1)$$

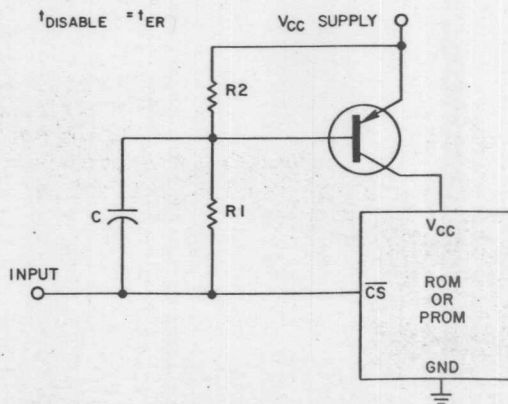
Notice that the turn-off time for the power switch in Fig. 2 is specified at 1.5 V, where most TTL PROMs are "off," and their outputs floating. If V_{CC} is dropped instantly to 1.5 V, the outputs will be "off" and floating within 10 ns. The worst-case disable time is thus given



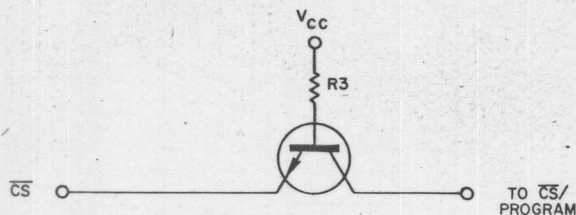
1. ROMs and PROMs are power-switched with a simple pnp transistor circuit in the V_{CC} line.



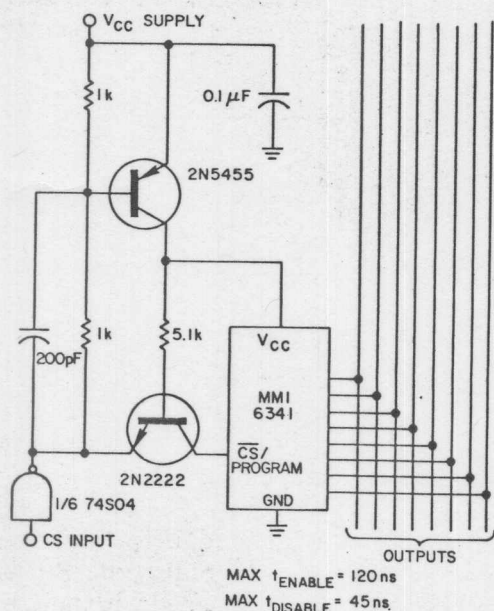
2. The output waveform of a pnp switch lags the input wave by t_{on} at the start, and by t_{off} at the end of the switching period.



3. Switching performance is improved with a speed-up capacitor, and in addition by feeding the switching input to the ROM's $\overline{CS}$ pin.



4. PROMs require an npn transistor at the $\overline{\text{CS}}$ /Program input to avoid excessive loading of the input wave.



5. The complete schematic for a PROM switch is developed for the 6341 PROM from Monolithic Memories.

Table 1. Suitable pnp switching transistors

No. of ROMs/PROMs	Some suitable pnp transistors
1	2N5455, 2N3467, 2N4402
2	2N3467, 2N3244
4	2N3467, 2N5023
8	2N3467

by the following equation:

$$t_{\text{disable}} = t_{\text{off(pnp)}} + 10 \text{ ns.} \quad (2)$$

The actual disable time can be quite long because $t_{\text{off(pnp)}}$ consists of two components: the turn-off time of the pnp transistor, and the decay time for V_{CC} . Because pnp transistors with good current-handling ability often have lousy turn-off times, you must be very careful to choose the right transistor for a pnp power switch. Several recommended transistors are listed in Table 1.

The decay time for V_{CC} depends on the current, I_{CC} , of the ROM or PROM. As V_{CC} approaches 1.5 V, I_{CC} drops very rapidly, and all or part of the current may turn on the output of the ROM. Accordingly, the $t_{\text{off(pnp)}}$ specified for the power switch may be quite high.

You can improve the performance of a pnp power switch in several ways. But two of the most effective are the following:

1. Use a speed-up capacitor in parallel with R_1 of the basic power switch in Fig. 1. This capacitor provides overdrive for turning the transistor on and off. The value should be such that the time constant, R_1C , is approximately equal to the fastest cycle time at which the power switch will be used. This technique, however, does not improve the decay time of V_{CC} .

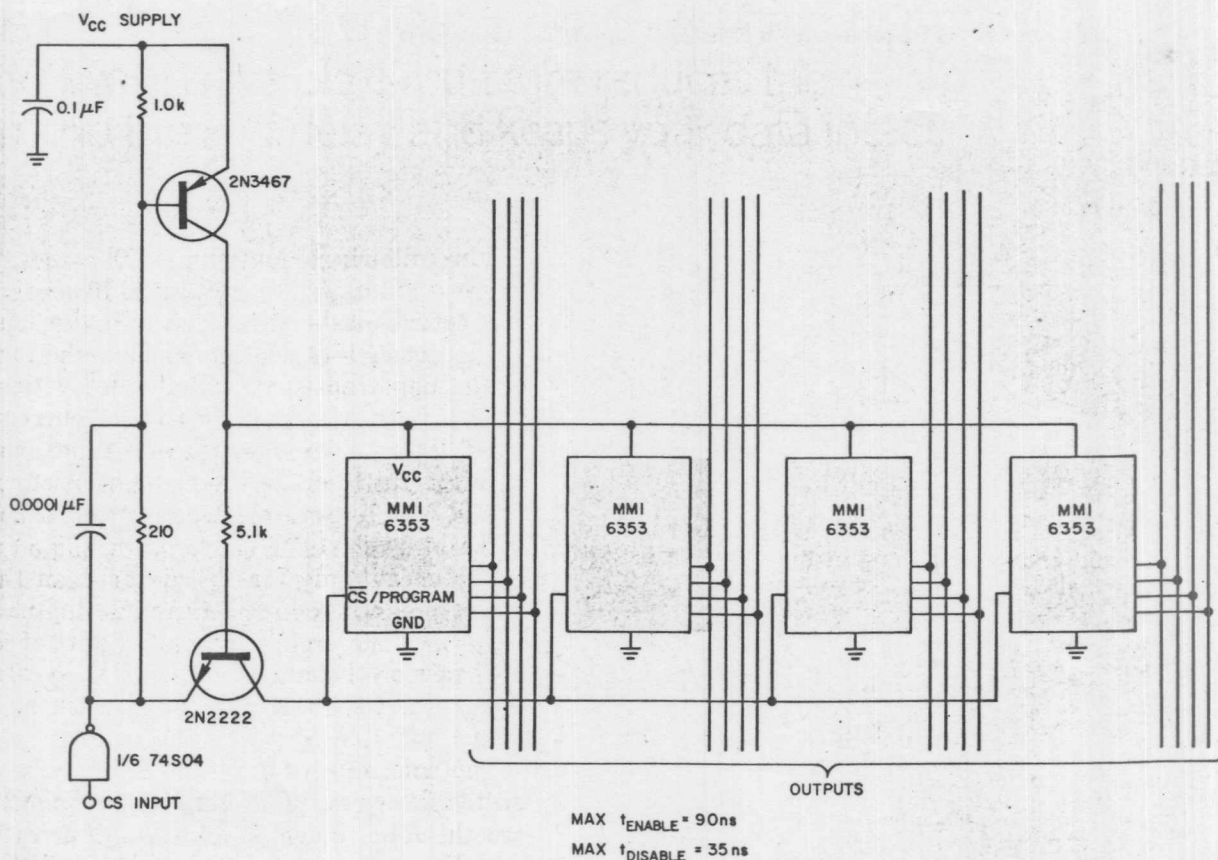
2. Tie the input of the power switch to a $\overline{\text{CS}}$ (chip enable) input of the ROM or PROM being switched. You thereby force the outputs into the OFF state as soon as the input to the power switch goes high. This means that while V_{CC} is decaying to 1.5 V, the outputs are held off, because the $\overline{\text{CS}}$ input is high. The internal $\overline{\text{CS}}$ buffer becomes ineffective when the outputs are turned off by V_{CC} .

With this second technique, the disable time is no longer represented by Eq. 2, but rather given by the t_{ER} time specified on the ROM or PROM data sheet:

$$t_{\text{disable}} = t_{\text{ER}}. \quad (3)$$

PROMs have special needs

What sets PROMs apart from ROMs is the fact that a $\overline{\text{CS}}$ input is also used as a programming input. The $\overline{\text{CS}}$ /Program input is designed in such a way that voltages higher than V_{CC} provide the internal currents necessary to program the device. Even at 5 V, this current can be very high. Consequently, when V_{CC} is



6. This example for power-switching a PROM array uses four MMI 6353 PROMs, for which the values of resistors

and capacitors are optimized. You should get a cycle time of approximately 1 μ s.

reduced by the power switch, the normal input-current spec does not apply. Instead, the $\overline{\text{CS}}$ /Program input and all signals tied in parallel with it are loaded down; while you expect a logic "1," it may be a "0."

This peculiarity can cause you headaches if you choose the $\overline{\text{CS}}$ /Program input in the improved switching scheme of Fig. 3. The loading of the $\overline{\text{CS}}$ /Program input is normally high enough to keep the input at a low level, and the pnp transistor remains on. Sometimes the whole system oscillates.

Fortunately, the following solution is simple, and works regardless of whether the $\overline{\text{CS}}$ /Program input is tied to a signal lead, or to the input of the power switch (Fig. 4): An npn transistor is used as a one-way switch to ensure that no current flows from the driver to the $\overline{\text{CS}}$ /Program pin. The small delay through the npn transistor can be ignored.

Here comes the new generation

The solution shown in Fig. 4 effectively changes the $\overline{\text{CS}}$ /Program input into a $\overline{\text{CS}}$ -only input. But you don't necessarily have to apply this solution in the case of

second or third-generation PROMs, which often have no $\overline{\text{CS}}$ /Program input. If the chip-enable pin does not have to go to a high level for programming, you can be sure that the npn transistor (Fig. 4) is not needed. A small memory like the MMI 5330/31 can do without the Program input. The MMI 5380/81, a 1-k $\times$ 8 bit configuration does not require the PROM solution either, because it was designed with power switching in mind: Zeners prevent the input circuit from being loaded down. If you want to power-switch PROMs, you really must know their design.

Even if your PROM turns out to be of an earlier variety, the outlined remedies work well. In Fig. 5, only one PROM is being switched with the concept described, while in Fig. 6, four PROMs are being switched. In both cases, the components give good operation in a system with a cycle time of 1 μ s.

The worst-case enable time in both cases is the t_{AA} from the data sheet, plus 30 ns. The worst-case disable time is t_{ER} from the data sheet. While the 2N2222 is used in Figs. 5 and 6, other transistors with fast turn-off time—like the 2N3444, 2N4275, and 2N5134—work just as well. ■